Recent Developments in Measurement and Metrology at ASML

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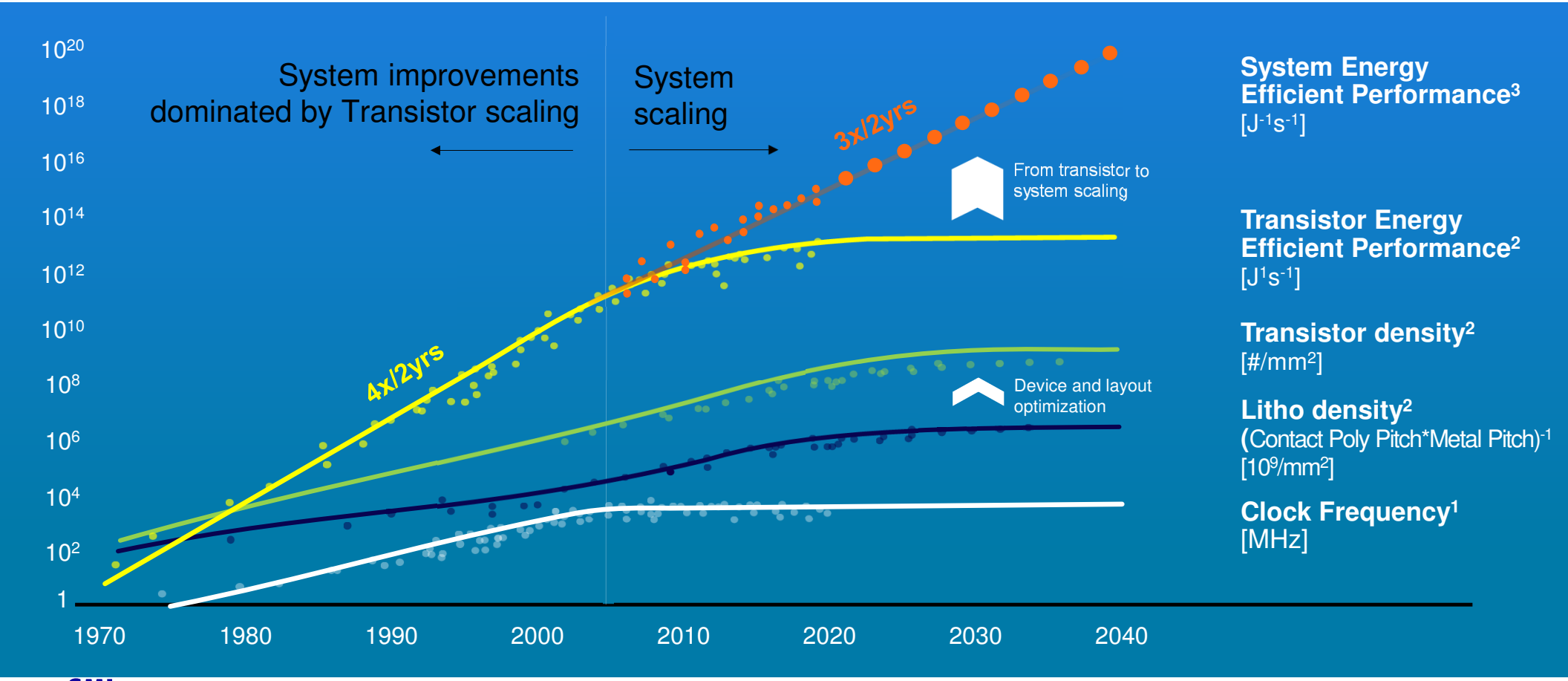
W3+ Fair Jena

Outline

- Moore’s law
- Metrology inside the scanner
  - Alignment sensor
  - Level sensor
- Metrology outside the scanner
  - Yieldstar
  - Digital Holographic Microscopy
- New Metrology concept for 3D measurements
- Conclusions

Moore's law evolution: the next 20 years

System scaling to satisfy the need for performance and energy consumption

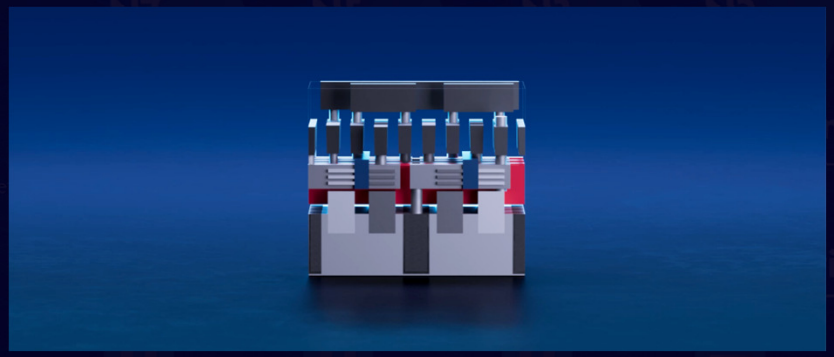


Sources: [1]Karl Rupp, [2] ASML data and projection using Rup, [3]Mark Liu TSMC normalized to transistor EEP in 2005

15 years of Logic device innovation and scaling ahead

Device roadmap is translated to litho requirements

Dimensional scaling continues, from Nanosheet to CFET

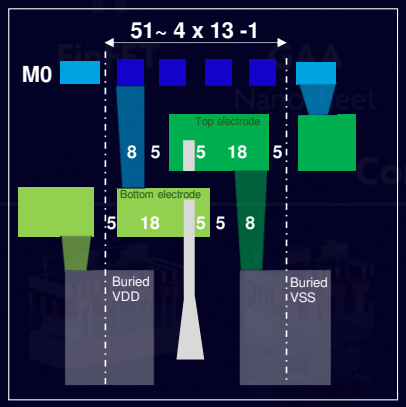


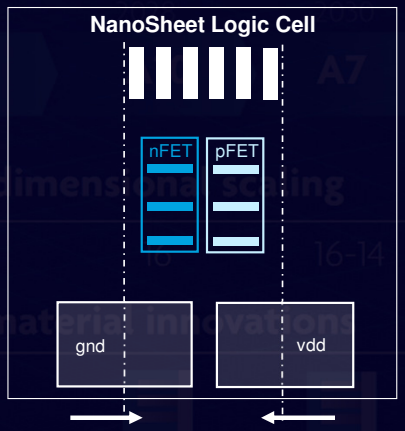
A5" node, HVM 2032

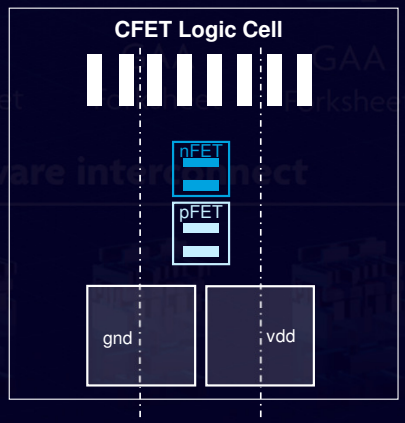
Cell Height ~50nm minimum

Connecting needs 3-4 tracks

Leads to 13nm pitch



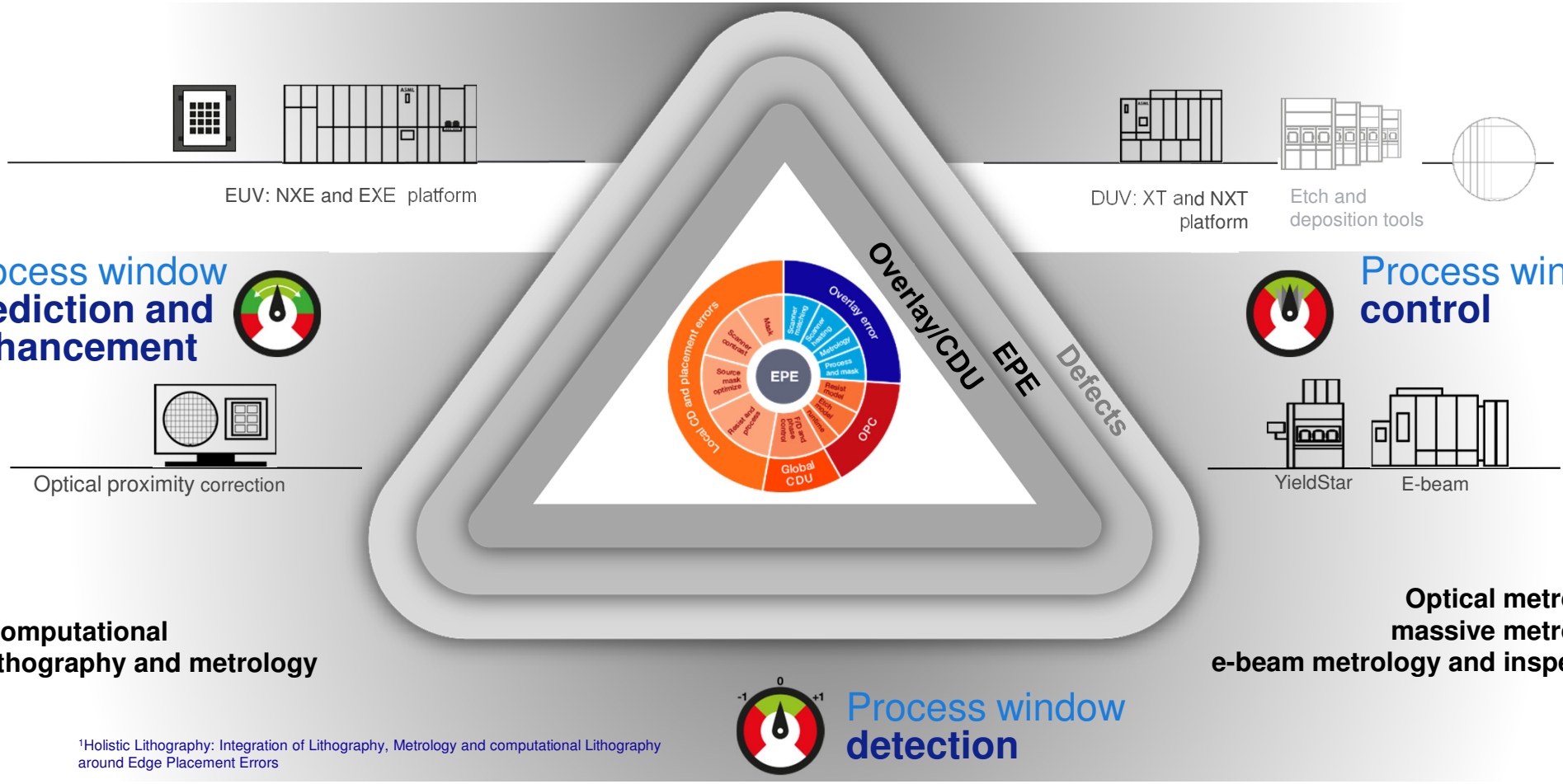




Source: Luc van den Hove, IMEC. "The endless progression of Moore's Law" ISS, April 2022

Holistic litho: Integration of Litho, Metro and Comp Litho around EPE[1]

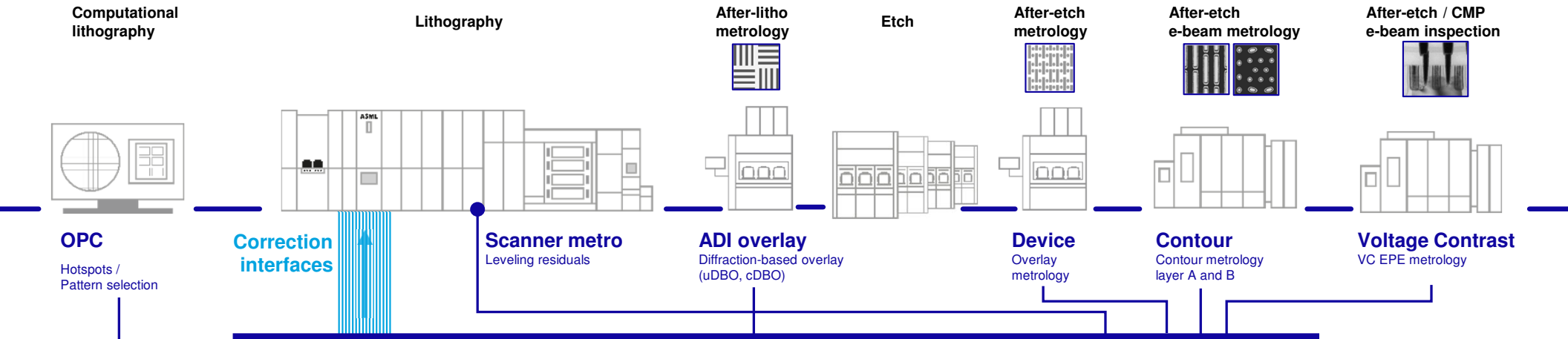
Lithography scanner with advanced control capability



[1]Holistic Lithography: Integration of Lithography, Metrology and computational Lithography around Edge Placement Errors

Holistic monitoring and optimization enabled by metrology and data platform

Combination of device overlay metrology and e-beam CD metrology data



Customer: Advanced Process Control, Fault Detection Control

Sub recipes to APC

Report KPIs to FDC

Litho InSight - Edge Placement Insight & Control

Full wafer EPE maps <2h AEI IDM & eP5 metrology and scanner corrections for EPE improvement

Enabled through a Virtual Computing Platform with controlled data access

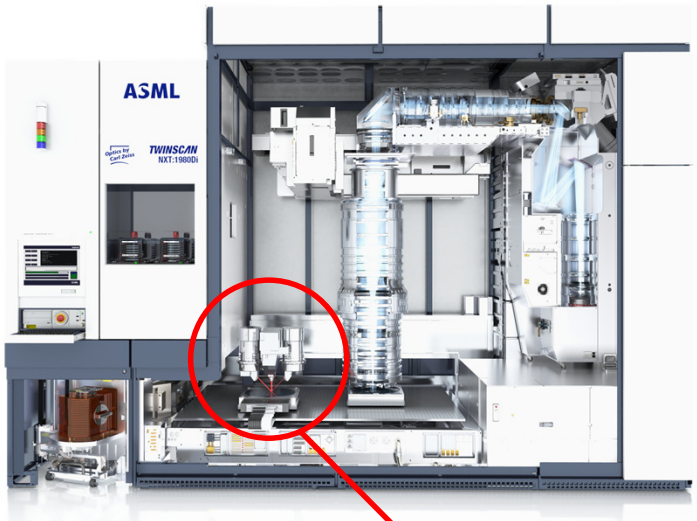
Metrology data

Corrections

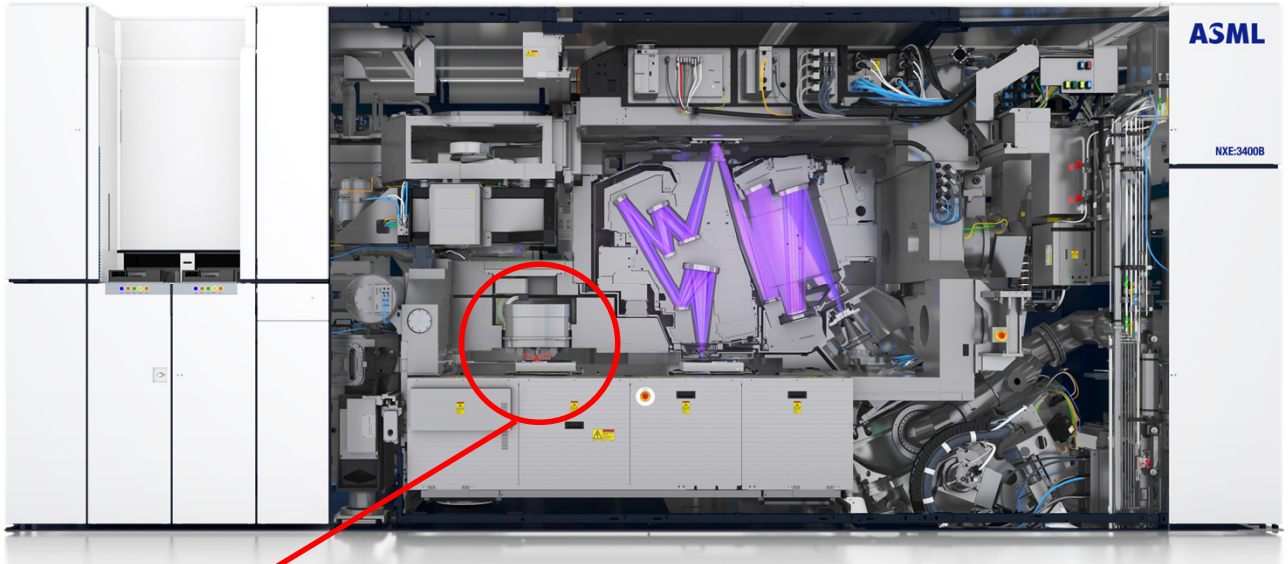
ASML

APC = Advanced Process Control, FDC=Fault Detection Control

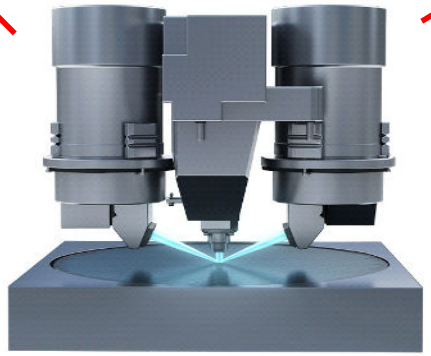
Optical Metrology in the Lithography Scanner



DUV – NXT systems



EUV – NXE systems



Measurement Systems for x-y-z Measurements
(Alignment & Level Sensor)

A lithography tool has 2 critical wafer-metrology sensors:

These sensors are used *before* the wafer is exposed

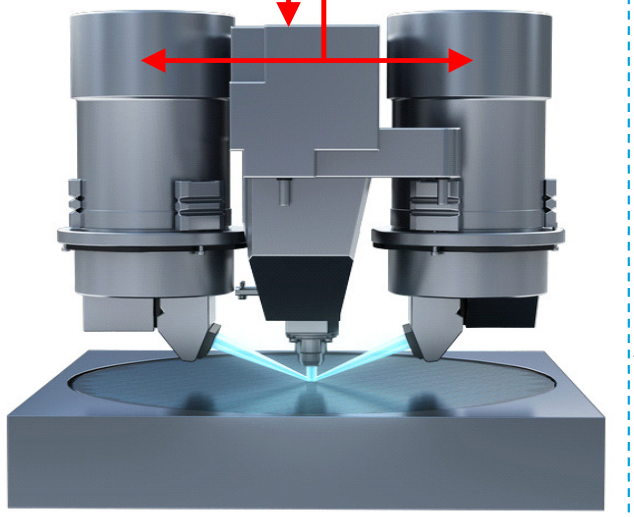
Alignment Sensor:
- Measures wafer *location*
- Critical for OV* performance

OV = overlay

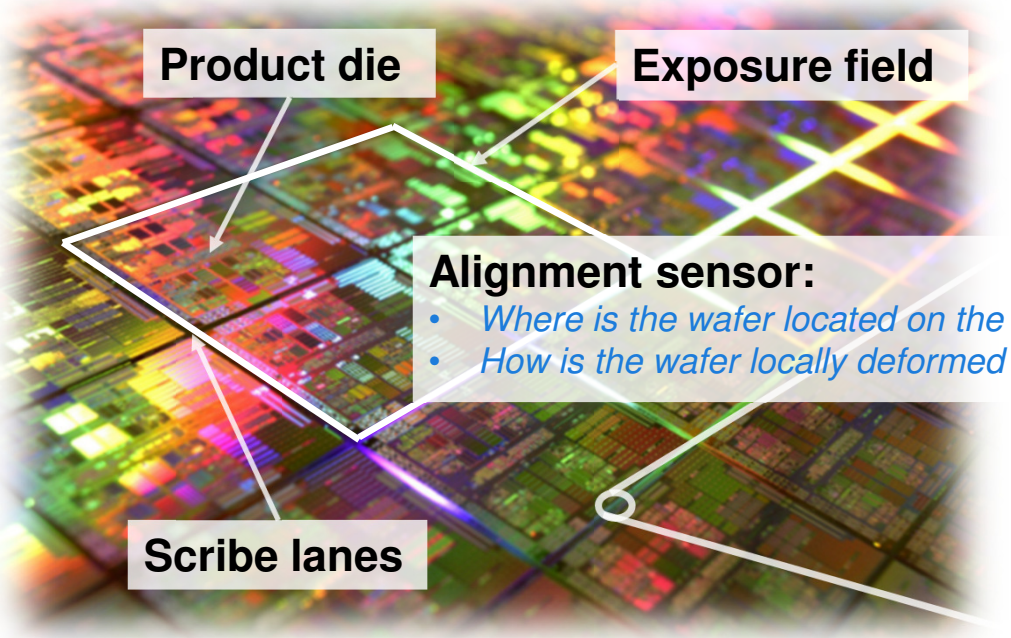
Level Sensor:
- Measures wafer *height*
- Critical for CDU* performance

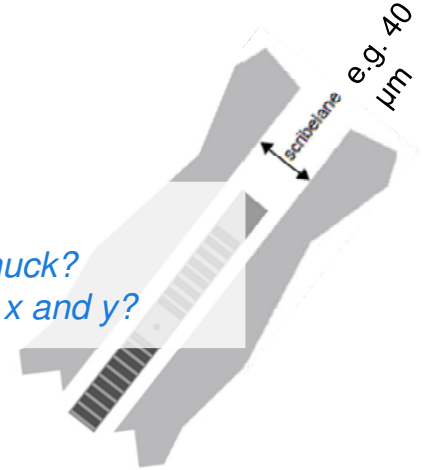
CDU = critical dimension uniformity

Boundary conditions:
- Phase-grating alignment
- Large dynamic range ~ 10^4
- Sub-nm accuracy
- Multiple wavelengths
- Flexibility in grating pitch
- Small spot : < 40 micron
- Working distance < 10mm



Alignment Sensor Challenges

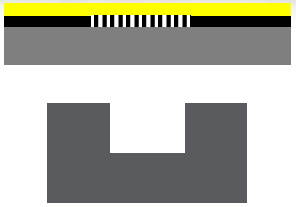




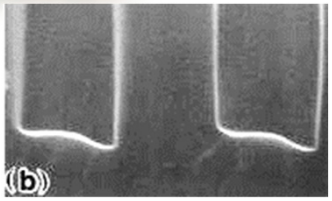
*Example of an **alignment** mark in a scribe **lane***

Goal:

- Alignment marks as small as possible
- With a pitch as small as possible (preferably similar to product features)
- Read out of 100+ marks per wafer (in ~5 seconds)



This is how we often draw an etched grating



In reality, grating profiles can be asymmetric as shown in this extreme example

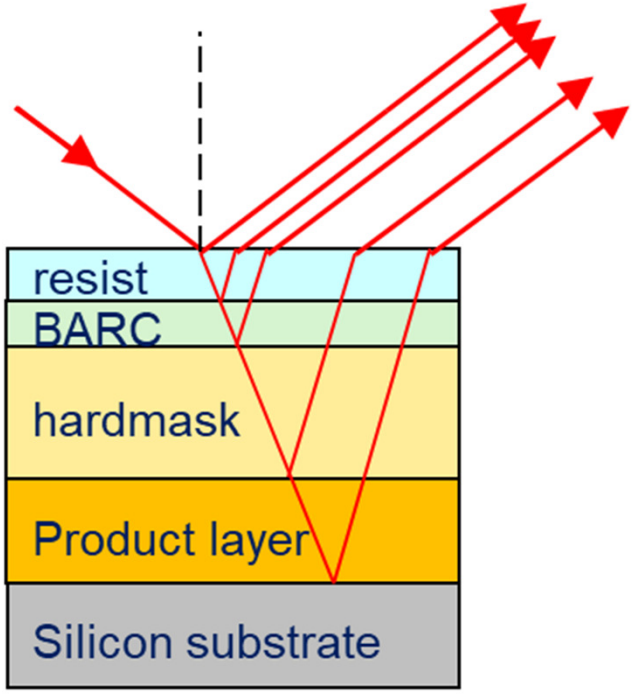
Etched grating profiles can also have asymmetric sidewalls due to "ion beam tilt"

Level Sensor Challenges

Level Sensor works with Triangulation principle

Goal:

- Make height map of full 300 mm wafer at a spatial resolution of ~0.5*1 mm (1e5 data points), to be able to print all features in focus
- At ~nm accuracy
- In ~1 second
- Be robust for process dependency
  - Hardmasks become thinner with new process nodes
  - Focus budgets become tighter, needing more accurate Level Sensor measurements

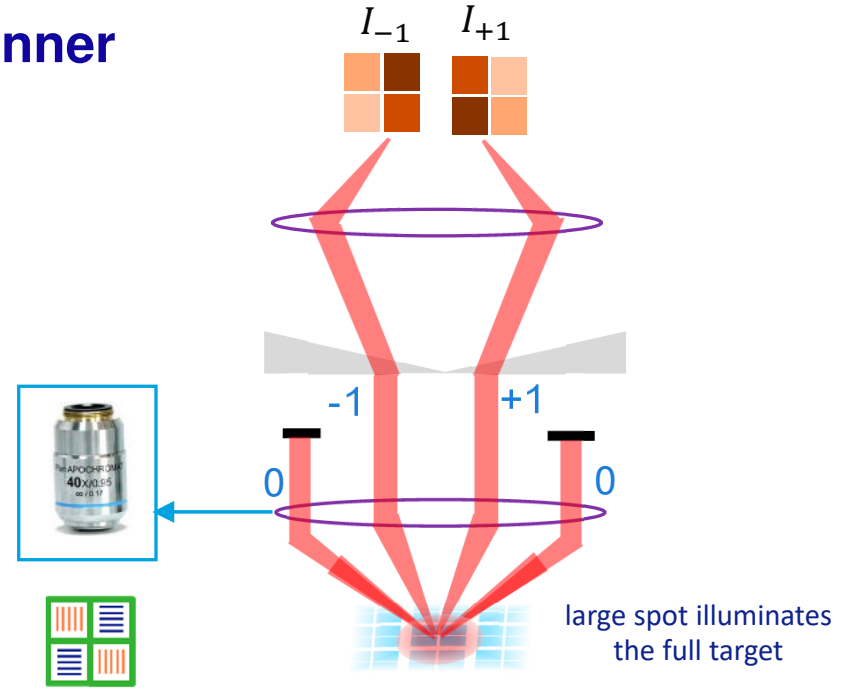


Layer thickness variations (and secondary reflections) can cause reflections from different interfaces in the stack, leading to offsets in measured height. These offsets vary with product layer variations.

Optical Metrology outside the Scanner

Yieldstar Optical Metrology

(Scatterometry sensor for Overlay Measurement, using dark field microscopy)

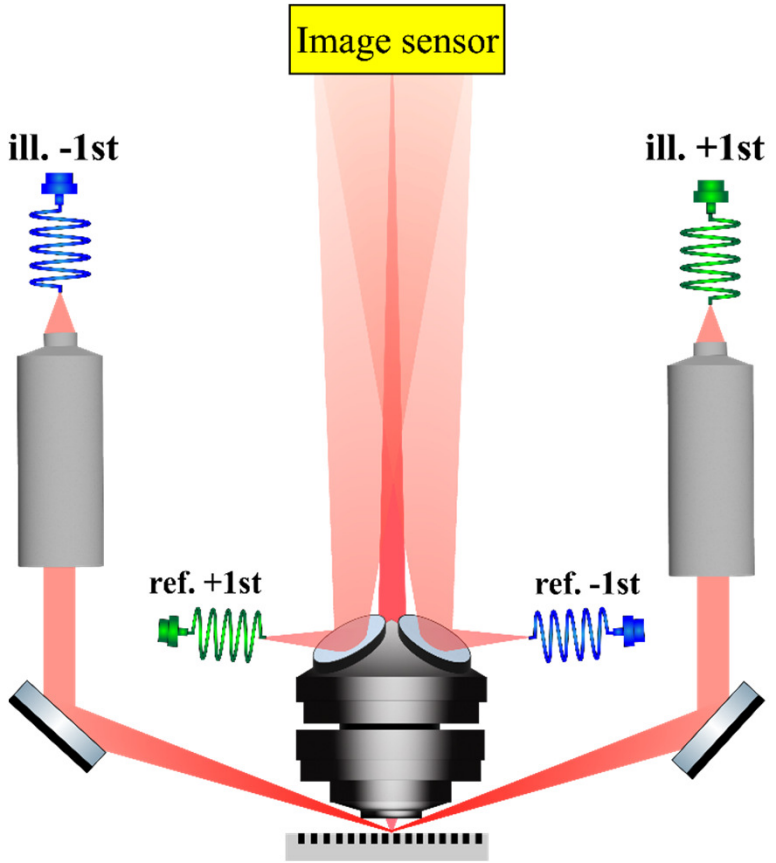


Goal:

- Overlay marks as small as possible
- With a pitch as small as possible (preferably similar to product features)
- Be robust for mark deformations
- Very fast readout (100s – 1000s marks per wafer)
- At low cost

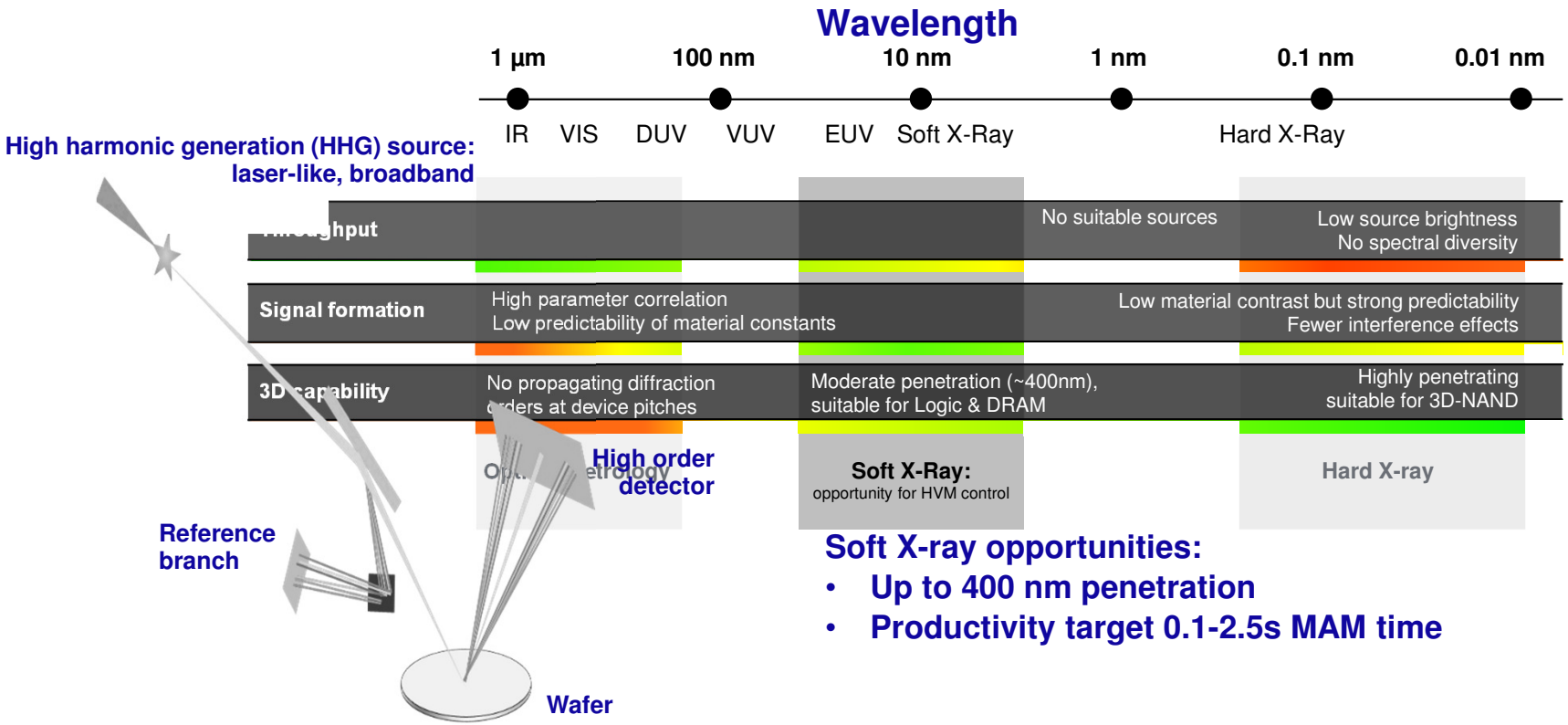
Potential Successor to Yieldstar – Digital Holographic Microscopy (DHM)

- Yieldstar optics become more complicated with each new generation
- DHM may offer a solution forward:
  - Simpler optics
  - Coherent illumination
  - Phase retrieval via digital holography
  - Strong computational correction possibilities
  - Simpler optics allow for more broadband use (towards the IR)



New 3D metrology tools needed to measure 3D structure with nm accuracy

Soft X-ray (10-20nm) metrology being explored by ASML



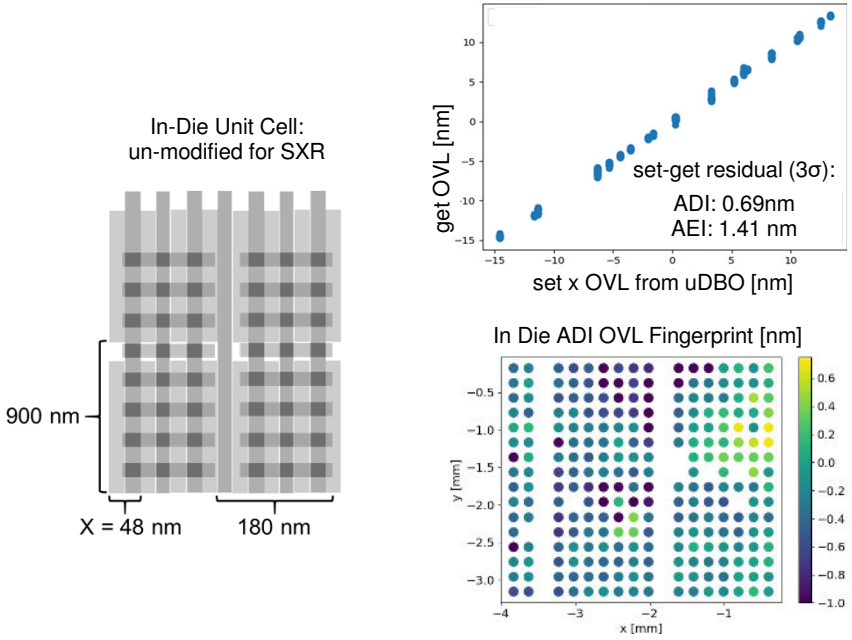
Soft X-ray opportunities:

- **Up to 400 nm penetration**
- **Productivity target 0.1-2.5s MAM time**

SXR demonstration of capabilities

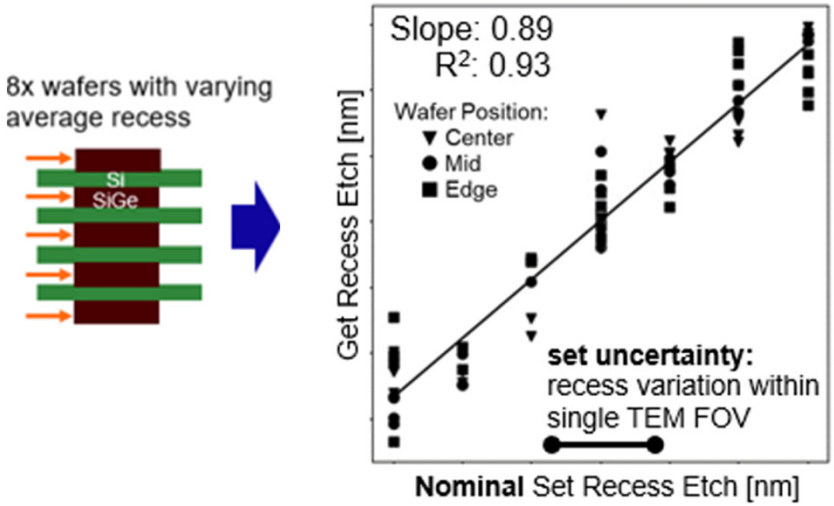
Joined Intel-ASML paper SPIE 2023

In Die overlay measurements



OVL sensitivity proven on **device pitch**, **in die area, despite underlying 3rd patterned layer** & coupon surface contamination.

3D / gate-all-aound Metrology Use Case



Set values are nominal based on etch time, horizontal bar shows recess etch variability within a single TEM field of view for these devices

Conclusions

- Moore's law is alive, but will be driven by more than just 2D scaling
- ASML's products require extensive metrology capabilities, both inside and outside the scanner
- Active research and product development is ongoing to develop the next generations of measurement systems
  - Alignment and Level Sensor inside the litho-scanner
  - Yieldstar, DHM and Soft X-Ray as stand-alone metrology tools
- In all these measurement systems optics plays a key role

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